REMARKS

Claims 1 to 3 have been examined. New claims 8 to 14 have been added. The new claims are supported by the original claims and the specification. No new matter has been added. Claims 4 to 7 have been canceled without prejudice. Therefore, claims 1 to 3 and 8 to 14 are pending.

Claim Rejections – 35 USC §112

Claims 1 to 3 have been rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The claims have been amended to address the indefinite rejection. No new matter has been added. Withdrawal of this rejection is respectfully requested.

Claim Rejections – 35 USC §103

Claims 1 to 3 have been rejected under 35 USC 103(a) as being unpatentable over Kadosh et al. in view of Wolf. Applicants respectfully submit that the invention according to claims 1 to 3 would not have been obvious to a person of ordinary skill in the art by the cited references for the following reasons.

Claim 1 recites:

> 1. (Amended) A semiconductor device comprising:
>
> a gate electrode formed on a first conductive type semiconductor substrate through a gate oxide film;
>
> **a first low concentration drain region of a second conductive type, provided at one end of said gate electrode;**
>
> **a second low concentration drain region of the second conductive type, provided in said first low concentration drain region, said second low concentration drain region being disposed close to an outer boundary of said first low concentration drain region and being higher in impurity concentration than at least an impurity concentration of the first low concentration drain region;**
>
> a high concentration source region of the second conductive type provided at another end of said gate electrode; and

> **a high concentration drain region of the second conductive type formed in said second low concentration drain region, said high concentration drain region being spaced away a predetermined distance from said gate electrode and being higher in impurity concentration than the second low concentration drain region**. (Emphasis added.)

The cited prior art references do not disclose, teach, or suggest the above bolded features. That is, Kodash et al. in view of Wolf does not describe a second low concentration drain region that is disposed **in** the first low concentration drain region and that is disposed close to an outer boundary of said first low concentration drain region, and a high concentration drain region that is disposed **in** the second low concentration drain region. This triple structure of the drain regions are not disclosed in Kadosh in view of Wolf.

Kadosh et al. teaches in FIG. 1O, a heavily doped source region 172 and ultra-heavily doped source region 186 merge to form a source, and lightly doped drain region 142 and heavily doped drain region 188 merge to form a drain for an NMOS device controlled by polysilicon gate 120. Heavily doped source region 172 provides a first channel junction 190 that is substantially aligned with sidewall 122, and lightly doped drain region 142 provides a second channel junction 192 that is substantially aligned with sidewall 124. In addition, ultra-heavily doped source region 186 and heavily doped drain region 188 are spaced from channel junctions 190 and 192. As it is clear from the description above, the heavily doped drain region 188 in not in the lightly doped drain region 142 but are disposed outside. This is clearly seen in Fig. 1O.

In the outstanding office action, it is stated that "Kadosh et al. lack anticipation only in not disclosing the following element: a second low concentration drain region." Applicants submit that not only Kadosh et al. lack a second low concentration drain region but also a high concentration drain region that is disposed **in** the second low concentration drain region. Thus, clearly, Kadosh et al. does not disclose a structure where a high concentration drain region that is within a second low concentration drain region that is within a first low concentration drain region.

Similarly, Wolf does not disclose, teach, or suggest a structure where a high concentration drain region that is within a second low concentration drain region that is within a

first low concentration drain region. Wolf's Fig. 9-46 shows a N- (As) region, a N- (P) region partially surrounding the N- (As) region, and a N+ (As) region adjacent to the N- (As) region. This structure is not the same as that claimed in claim 1 as indicated above.

Thus, for the foregoing reasons, the present invention according to claim 1 is not disclosed, taught, or suggested by the cited prior art references.

Furthermore, claims 2 and 3 which depend on claim 1 are not obvious at least for the same reason as claim 1.

New Claims

New claim 8 also depends on claim 1. Thus, at least for the same reason as claim 1, claim 8 is not obvious.

New independent claim 9 has similar features as claim 1. Claim 9 recites:

> 9. (New) A semiconductor device comprising:
> a semiconductor substrate;
> an gate oxide film provided on the semiconductor substrate;
> a gate electrode disposed on the gate oxide film;
> **a first drain region provided at one end of said gate electrode in the semiconductor substrate;**
> **a second drain region provided in said first drain region, an outer boundary of said second drain region being disposed close to an outer boundary of said first drain region;**
> **a third drain region provided in said second drain region, said third drain region being spaced away a predetermined distance from said gate electrode and being spaced far apart from the outer boundary of the second drain region**; and
> a region of the second conductive type provided at another end of said gate electrode,
> wherein the first, second, and third drain regions all having different impurity concentrations.
> (Emphasis added.)

At least the above bolded features are not disclosed, taught, or suggested by the cited prior art. Dependent claims 10 to 14 are not obvious at least for the same reasons.

Thus, for the foregoing reasons, Applicants submit that all pending claims are allowable over the cited prior art references.

Attached is a marked-up version of the changes being made by the current amendment.

Applicant asks that all claims be allowed. Enclosed is a check for excess claim fees and a check for the Petition for Extension of Time fee (one month). Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: 1/13/03

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Version with markings to show changes made

In the specification:

A substitute specification is provided herein. No new matter has been added.

In the claims:

Claims 4 to 7 have been canceled without prejudice.

Claims 1 to 3 have been amended as follows:

1. (Amended) A semiconductor device comprising:

a gate electrode formed on a first conductive type semiconductor substrate [via] through a gate oxide film;

a first low concentration drain region of a second conductive type, [being formed adjacent to] provided at one end of said gate electrode;

a second low concentration drain region of the second conductive type, [being formed] provided in said first low concentration drain region, [so that] said second low concentration drain region [is very] being disposed close to an outer boundary of said first low concentration drain region[,] and being higher in impurity concentration than at least an impurity concentration of the first low concentration drain region; [and]

a high concentration source region of the second conductive type [which is formed adjacent to] provided at another end of said gate electrode; and

a high concentration drain region of the second conductive type [which is] formed in said second low concentration drain region, said high concentration drain region being spaced away [having] a predetermined distance from [the one end of] said gate electrode and being higher in impurity concentration than the second low concentration drain region.

2. (Amended) A semiconductor device according to Claim 1, wherein said first low concentration drain region and said second low concentration drain region are formed by utilizing two kinds of second conductive type impurities, and [each of] the two kinds of said

second type conductive impurities [has a] have different diffusion coefficients [different from each other].

3. (Amended) A semiconductor device according to Claim 1, wherein said first low concentration drain region and said second low concentration drain region are formed by using [a first impurity consisting of] phosphorus ions and [a second impurity consisting of] arsenic ions, respectively.

In the Abstract:

The abstract has been amended as follows:

[The objective of the present invention is to improve drain withstanding voltage at operation.]

A semiconductor device [of the present invention] has a gate electrode [9]formed on a P type semiconductor substrate ~~1~~ via gate oxide films. [7A and 8, a] A first low concentration (LN type) drain region[-5 being]is made adjacent to one end of the gate electrode. [9, a] A second low concentration (SLN type) drain region [6 which] is formed ~~a~~ in the first low concentration drain region [5] so that [said] the second low concentration drain region [6] is very close to the outer boundary of [said] the second low concentration drain region [5] and [is] has at least a higher [in] impurity concentration than [that of] the first low concentration drain region. [5 a] A high concentration (N+ type) source region [10] is formed adjacent to the other end of said gate electrode [9], and a high concentration (N+ type) drain region [11] is formed in [said] the second low concentration drain region [10] having the designated space from one end of [said] the gate electrode [9].

Substitute Specification
Marked-Up Copy

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

1.Field of the Invention

The present invention relates to a semiconductor device and a method for manufacturing the semiconductor device, particularly to a technique of improving withstanding operating voltage~~ while depressing decrease of driving ability~~.

2.Description of the Related Art

Fig. 5 is a sectional view describing ~~the~~ a conventional semiconductor device.

In Fig. 5, symbol 51 ~~is~~ refers to a first conductive~~, for example~~ P type~~,~~ semiconductor substrate.~~,~~ ~~o~~On the substrate 51, a gate electrode 53 is formed through a gate oxide film 52, and a source-drain region of a one-~~-~~sided LDD (Lightly Doped Drain) structure is formed ~~so as to be~~ adjacent to the gate electrode 53. That is, this ~~a~~ semiconductor device ~~having~~ has a source-drain region of the one-~~-~~sided LDD structure. ~~in which~~ A high concentration (N+

type) source region 55 is formed at the source region side ~~so as to be~~ adjacent to ~~said~~the gate electrode 53, a low concentration (N- type) drain region 54 is formed at the drain region side ~~so as to be~~ adjacent to said gate electrode 53, and a high concentration (N+ type) drain region 56 is formed in the low concentration drain region 54.

As described above, in the semiconductor device of the one- sided LDD structure in which a high voltage is applied only to the drain region side, the high concentration drain region 56 is surrounded ~~with~~ by the low concentration drain region 54 to defuse concentration of electric field in the drain region side, as ~~above-mentioned~~mentioned above. However, in the source region side, only the high concentration source region 55 exists.

Even the semiconductor device having such ~~the~~ a structure is needless to take its structure as a particular problem with regard to static withstanding voltage. However, at operation, the following problem occurs.

That is, in a bipolar structure consisting of a source region (emitter region), a substrate (base region), and a

drain region (collector region), injection efficiency of carrier is good because a high concentration source region 55 is exposed in emitter region, so that the bipolar ~~transistor~~ structure ~~is~~ can be made ~~on~~ easily by a little substrate current Isub.

That is, since current gain βin the bipolar ~~transistor~~structure with a one-sided LLD structure is high, the drain withstanding voltage ~~at operation~~during operation decreases ~~comparing~~ compared with a semiconductor device of ~~both~~ a double-sided~~s~~ LDD structure.

Here, in order to improve the drain withstanding voltage ~~at operation~~during operation, ~~it needs to decrease~~ the substrate current Isub needs to be decreased. That is, ~~it needs to make further drain~~ the electric field must be made weak.

However, when an impurity concentration of the entire~~whole~~ low concentration drain region 54 is ~~made thin~~ decreased in order to decrease the substrate current Isub, the substrate current Isub has a double hump structure having two peaks ((1) and (2)) as voltage Vg increases, as shown in Fig. 6.

When the low concentration drain region 54 is further ~~low~~decreased, the first peak (1) of the substrate current Isub is low so that the drain withstanding voltage at low Vgs improves. However, the second peak (2) of the substrate current Isub is comparatively high so that drain withstanding voltage at high Vgs decreases.

Conversely, when ~~whole~~ the entire impurity concentration of the low concentration drain region 54 is high, ~~one~~ a single peak ~~having~~ at a certain voltage Vgs appears ~~so as to be useful for~~and the drain withstanding voltage at high Vgs decreases, as shown in Fig. 6. However, there is a problem that the drain withstanding voltage at low Vgs can not withstand.

Thus, when ~~whole~~ the entire impurity concentration of the low concentration drain region 54 is changed uniformly, the change can not ~~get out of~~overcome the trade-off relationship of the drain withstanding voltage at low Vgs and the drain withstanding voltage at high Vgs.

Although current gain β decreases and the withstanding voltage withstands decidedly by adopting ~~both sides~~a double-sided LDD structure ~~generally used~~, the device has distance

(L) of a drift region similar ~~as~~ to the drain side shown in Fig. 5.~~,~~ In this instance, ~~so that~~the on-resistance increases and the driving ability decreases because a usual LDD structure is adopted at the source side, ~~in spite of no need of~~ although the withstanding voltage at the source side is not needed.

SUMMARY OF THE INVENTION

The invention ~~carried out in view of the above-mentioned problems~~ is a semiconductor device comprising: a gate electrode formed on a first conductive type semiconductor substrate via a gate oxide film; a first low concentration drain region of a second conductive type, being formed adjacent to one end of ~~said~~the gate electrode; a second low concentration drain region of the second conductive type, being formed in ~~said~~ the first low concentration drain region so that ~~said~~ the second low concentration drain region is very close to the outer boundary of ~~said~~the first low concentration drain region, and being higher in impurity concentration than at least impurity concentration of the first low concentration drain

region; and a high concentration source region of the second conductive type being formed adjacent to another end of ~~said~~the gate electrode and a high concentration drain region of the second conductive type being formed in ~~said~~the low concentration drain region having a predetermined distance from the one end of ~~said~~the gate electrode.

A method for manufacturing a semiconductor device comprises: a first process comprising steps of a first step forming a first photo resist film having a first opening at a drain forming region on a first conductive type semiconductor substrate, a second step ion-implanting a first impurity of the second conductive type and a second impurity of the second conductive type with the first photo resist film being used as a mask, and a third step forming a first low concentration drain region of the second conductive type and a second low concentration drain region of second type by diffusing ~~said~~the first impurity and ~~said~~the second impurity after the fore-mentioned ion-implanting step; a second process forming an element separation film at a predetermined region by selectively oxidizing with an oxidization resist film formed on ~~said~~the

substrate as a mask and forming a second gate oxide film at region except the element separation film and the first gate oxide film; a third process forming a gate electrode so as to cover from ~~said~~the first gate oxide film to the second gate oxide film; a fourth process forming a second photo resist film having a second opening on the source forming region on ~~said~~the substrate and having a third opening on a region separated from another end of ~~said~~the gate electrode on ~~said~~the low concentration drain region; and a fifth process forming high concentration source-drain regions of the second conductive type by ion-implanting a third impurity of the second conductive type on ~~said~~the substrate with ~~said~~the second photo resist film, ~~said~~the gate electrode, ~~said~~the element separation film, and ~~said~~the first gate oxide film as a mask.

Thus, the second low concentration drain region higher in impurity concentration than impurity of the first low concentration drain region is formed in ~~said~~the first low concentration drain region of second conductive type so that ~~said~~the second low concentration drain region is very close to the outer boundary of ~~said~~the first low concentration

drain region. By that, the low concentration drain region is made with a double structure consisting of two kinds of impurity ions different in diffusion coefficient without uniformly changing impurity distribution in the low concentration drain region. Therefore, the first low concentration drain region withstands low Vgs withstanding voltage, and the second low concentration drain region withstands high Vgs withstanding voltage.

Further, the process forming ~~said~~the first low concentration drain region and second low concentration drain region have a process thermal-treating, at the same time, ~~said~~the first impurity consisting of phosphorus ion and ~~said~~the second impurity consisting of arsenic ion and use difference of diffusion coefficients of these impurities.

Thus, since difference of diffusion coefficients of two kinds of impurities is used and these impurities are formed at the same process when the first low concentration drain region and the second low concentration drain region are formed, the second low concentration drain region can be formed accurately at very near part in the first low

concentration drain region.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing a method for manufacturing a semiconductor device according to ~~the mode for carrying out~~ an embodiment of the invention.

Fig. 2 is a sectional view showing a method for manufacturing a semiconductor device according to ~~the mode for carrying out~~ an embodiment of the invention.

Fig. 3 is a sectional view showing a method for manufacturing a semiconductor device according to ~~the mode for carrying out~~an embodiment of the invention.

Fig. 4 is a sectional view showing a method for manufacturing a semiconductor device according to ~~the mode for carrying out~~an embodiment of the invention.

Fig. 5 is a sectional view showing ~~the~~ a conventional semiconductor device.

Fig. 6 ~~is a view describing the conventional problem~~ graphically shows a problem in connection with the device shown in Fig. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

An embodiment of a semiconductor device of the present invention and a method for manufacturing the semiconductor device according to the present invention will be described referring to figures.

In ~~the~~ a semiconductor device according to the invention, a gate electrode 9 is formed on a P type substrate, for example, a semiconductor substrate 1 ~~so as to cover~~and disposed over from a first gate oxide film 7A to a second gate oxide film 8, as shown in Fig. 4.

A high concentration (N+ type) source region 10 is formed ~~so as to be~~ adjacent to one end of ~~said~~the gate electrode 9 (one end of the second gate oxide film 8). Further, a first low concentration (LN type) drain region 5 is formed ~~so as to be~~ adjacent to the other end of ~~said~~the gate electrode 9 (the other end of the first gate oxide film 7A).~~, and a~~ A second low concentration (SLN type) drain region 6 at least higher in impurity concentration than ~~impurity of~~ the first low concentration (LN type) drain region 5 is formed in the first low concentration (LN type) drain region 5 so that the second low concentration drain

region 6 is very close to the outer boundary of the first low concentration drain region 5. Further in the drain region 6, a high concentration (N+ type) drain region 11 is formed at a region separated from ~~said~~the gate electrode 9 (so as to be adjacent to one end of ~~said~~the first gate oxide film 7A).

~~Adopting such the construction,~~ Thus, the second low concentration (SLN type) drain region 6 higher in impurity concentration than ~~impurity of~~ the first low concentration (LN type) drain region 5 is formed in ~~said~~the first low concentration (LN type) drain region so that ~~said~~the second low concentration drain region 6 is very close to the outer boundary of ~~said~~the first low concentration drain region 5. By that, a low concentration drain region is made with a double structure consisting of two kinds of impurity ions ~~different~~ differing in diffusion coefficient.~~, t~~ That is, the drain region has ~~covering thinly~~ the second low concentration (SLN type) drain region 6 ~~higher in impurity concentration than impurity of the first low concentration (LN type) drain region 5~~ thinly covering ~~with~~ the first low concentration (LN type) drain region 5, without changing

uniformly the impurity distribution in the low concentration drain region~~ conventionally~~. Therefore, the first low concentration (LN type) drain region 5 withstands a low Vgs withstanding voltage, and the second low concentration (SLN type) drain region 6 withstands a high Vgs withstanding voltage ~~so as~~ to improve the drain withstanding voltage ~~at operation~~during operation.

Thus, by the construction ~~that~~ of the low concentration drain region ~~has~~ with two or more kinds of different impurity concentrations, and ~~not~~ by not changing the impurity distribution uniformly over ~~whole~~ the entire low concentration drain regions, the drain withstanding voltage ~~at operation~~during operation can be improved ~~with independence~~independent of the trade-off relationship of drain withstanding voltage at low Vgs and the drain withstanding voltage at high Vgs.

~~Since it is needless~~ Because there is no need to adopt the conventional semiconductor device of the LDD structure having substantially symmetrical~~y~~ low concentration source-drain regions in the source-drain regions and because the device according to the present invention does not have a

drift region compared~~ing~~ with the conventional semiconductor device, ~~decrease of~~ the driving ability ~~can be~~is not suppressed~~depressed~~.

A method for manufacturing the above-mentioned semiconductor device will be described below referring to the figures.

First, in Fig. 1, a photo resist (PR) film 2 having an opening on a drain forming region on a P type semiconductor substrate 1 is formed, ~~with~~ while using the photo resist (PR) film 2 as a mask.~~, and f~~ First and second impurity implantation regions are formed by ion-implanting first and second impurities. ~~At this time, said~~The second impurity is required to ~~be an impurity less in~~ have a diffusion coefficient less than ~~said~~the first impurity.~~, and when said~~ If the first impurity is phosphorus-ion, the second impurity can be arsenic-ion, for example~~, is used for the second impurity~~. After a first impurity implantation region 3 is formed by ion-implanting phosphorus-ions with an acceleration voltage of 100 KeV ~~and~~ at a dose of about 6 x $10^{12}/cm^2$, a second impurity region 4 is formed by ion-

implanting arsenic-ions with an acceleration voltage of 160 KeV ~~and~~ at a dose of about 5 x $10^{11}/cm^2$.

Next, in Fig. 2, after removing ~~said~~the photo resist film 2, a first low concentration (LN type) drain region 5 is formed by thermally -diffusing ~~said~~the phosphorus ions and arsenic ions.~~, and a~~ A second low concentration (SLN) drain region 6 with higher ~~in~~ impurity concentration than at least the low concentration drain region 5 is formed in the low concentration drain region so that the second low concentration drain region 6 is very close to the outer boundary of the first low concentration drain region 5. At this time, a thermal treatment of about 1100 □ and 4 hours is carried out ~~in this embodiment~~.

In the process, two kinds of impurity ions (phosphorus ~~ion~~ and arsenic ~~ion~~) having different ~~in~~ diffusion coefficients are ion-implanted using the same mask (photo resist film 2) and diffused using the difference in~~of~~ diffusion coefficients ~~of these impurities~~. ~~Because of that~~Thus, the second low concentration (SLN type) drain region 6 with comparatively high ~~in~~ impurity concentration can be formed ~~so as to be covered~~ with the thin first low

concentration (LN type) drain region 5 ~~with~~ suitablye spaced apart.

Next, in Fig. 3, after forming a pad oxide film and a silicon nitride film as an oxidation resistance film having an opening at the designated region (a first gate oxide film forming region and an element separation film forming region) not shown on ~~said~~the substrate 1, a first gate oxide film 7A and an element separation film 7B of about 1000 nm thickness are formed by using the silicon nitride film as a mask and oxidizing the oxidation resistance film selectively by a known LOCOS method. Further, after removing ~~said~~the pad oxide film and silicon nitride film, a second gate oxide film 8 of 150 nm thickness is formed by thermal-oxidizing ~~on~~ the substrate where ~~said~~the first gate oxide film 7A and element separation film 7B are not formed. Then, after a polysilicon film of 400 nm thickness is formed on ~~said~~the substrate 1 and ~~carrying out~~ a conducting treatment of the polysilicon film is carried out, a gate electrode 9 is formed ~~so as~~ to ~~cover~~ dispose over from ~~said~~the first gate oxide film 7A to the second gate oxide film 8, patterning a photo resist film, not shown, which is used as a mask. At

this time, the second gate oxide film 8 on the substrate 1 except the part where the ~~gate oxide film 8~~gate electrode 9 is formed is removed.

Further, in Fig. 4, an N type impurity is ion-implanted ~~so as~~ to be adjacent to one end of ~~said~~the gate electrode 9 using a photo resist (PR) film 12 formed on ~~said~~the substrate 1 as a mask. An ~~I~~ion-implanting N type impurity ~~so as to separate from~~ is also deposited at the other end of ~~said~~the gate electrode 9 ~~and~~ to be adjacent to one end of ~~said~~the gate oxide film 7A.~~, a~~ That is, a high concentration (N+ type) source region 10 is formed ~~so as~~ to be adjacent to one end of ~~said~~the gate electrode 9. Then, a high concentration (N+ type) drain region 11 is formed at a region separated from the other end of ~~said~~the gate electrode 9 (~~so as~~ to be adjacent to the other end of ~~said~~the first gate oxide film 7A) in ~~said~~the second low concentration drain region 6. At this time, arsenic ions ~~is~~ are ion-implanted with an acceleration voltage of about 80 KeV ~~and~~ at a dose ~~implanting quantity~~ of about 6 X $10^{15}/cm^2$.

Although description shown in the figure is omitted, source-drain electrodes are formed through contact holes

after forming an insulation film between layers over whole surface forming the contact holes on the insulation film between layers ~~so as~~ to make contact with ~~to said~~the source-contact regions.

Thus, in the method for manufacturing the semiconductor device of the present invention, two kinds of impurities (phosphorus ~~ion~~ and arsenic ~~ion~~), which are ion-implanted previously on the surface of ~~said~~the substrate and ~~are~~ have different ~~in~~ diffusion coefficients, are treated ~~with thermal~~thermally to induce diffusion. Using the difference ~~of~~ in the diffusion coefficients, a low concentration drain region of a double structure having two kinds of impurity concentration is formed. That is, the low concentration drain region is formed ~~so as~~ to cover thinly the second low concentration (SLN type) drain region 6 (based on arsenic ions) with the first low concentration (LN type) drain region 5 (based on phosphorus ions). Therefore, ~~differing from~~in contrast to changing impurity concentration uniformly over the whole low concentration drain regions ~~as conventionally~~, the drain withstanding voltage ~~at operation~~during operation can be improved ~~with independence~~

~~of~~independent of any trade-off relationship of drain withstanding voltage at a low Vgs and drain withstanding voltage at a high Vgs.

According to the invention, by forming a low concentration drain region ~~so as~~ to have two kinds of different impurity concentrations, the low Vgs withstanding voltage withstands at ~~a~~ the first low concentration drain region ~~low in impurity concentration withstands~~, and the high Vgs withstanding voltage withstands at ~~a~~ the second low concentration drain region ~~high~~ so as to improve the drain withstanding voltage characteristics ~~at operation~~during operation.

~~Because t~~The first low concentration drain region and the second low concentration drain region are formed ~~using difference of the diffusion coefficients by thermal treatment of~~ by thermally treating the two kinds of implanted impurities having ~~which are previously ion-implanted to surface of a substrate and are~~ different ~~in~~ diffusion coefficients.~~,~~ Thus, the second low concentration drain can be formed in the first low concentration drain region so that ~~said~~the second low concentration drain is

very close to the outer boundary of ~~said~~the first low concentration drain region.